DATA SHEET

TDA7057AQ
2 x 5 W stereo BTL audio output amplifier with DC volume control

Preliminary specification
Supersedes data of July 1994
File under Integrated Circuits, IC01

1995 Nov 08

Philips Semiconductors

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FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is a stereo BTL output amplifier with DC volume control. The device is designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_P = 12 V; R_L = 16 Ω	3.0	3.5	–	W
		V_P = 12 V; R_L = 8 Ω	–	5.3	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_P = 12 V; $R_L = \infty$	–	22	25	mA
THD	total harmonic distortion	P_{out} = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7057AQ	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

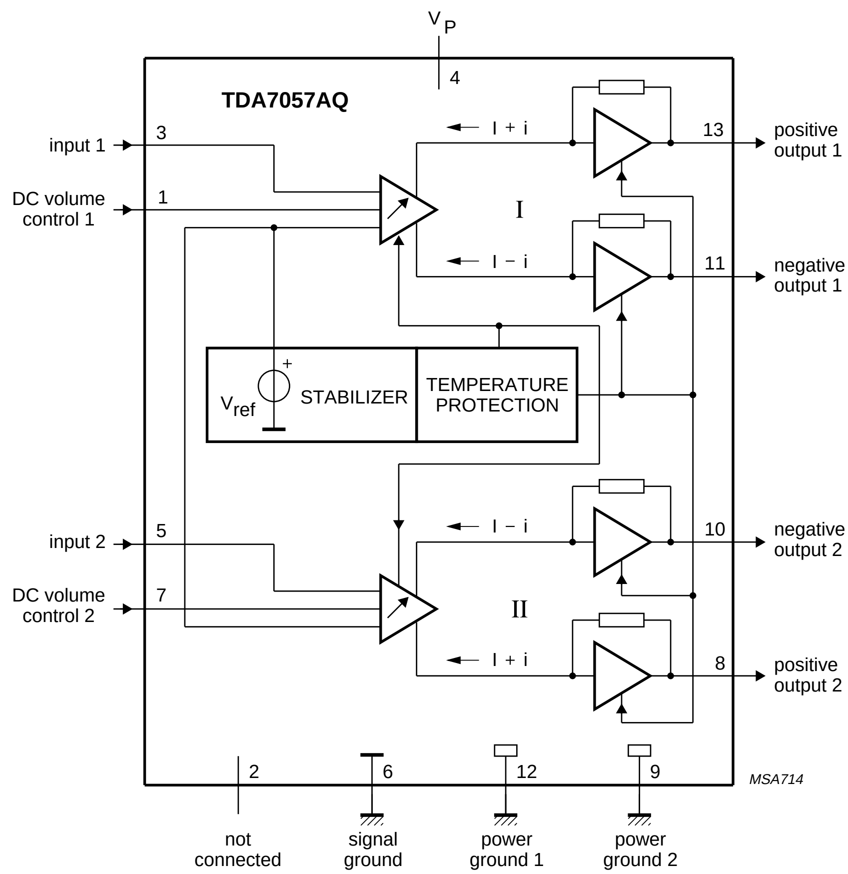


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c.	2	not connected
$V_{I(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2–	10	negative output 2
OUT1–	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

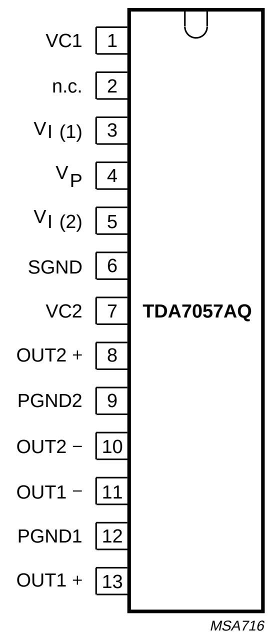


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7057AQ is a stereo output amplifier with two DC volume control stages. The device is designed for TV and monitors, but are also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

In the TDA7057AQ the two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages;

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 dB to –33 dB. If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is a short-circuit protected to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.

Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{case} < 60 °C	–	22.5	W
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
t_{sc}	short-circuit time		–	1	hr
V_n	input voltage pins 1, 3, 5 and 7		–	5	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	4	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	40	K/W

Power dissipation

Assume V_P = 12 V and R_L = 16 Ω. The maximum sine wave dissipation is 2 × 1.8 W = 3.6 W.

At $T_{amb\ (max)}$ = 60 °C;

$R_{th\ tot}$ = (150 – 60)/3.6 = 25 K/W

$R_{th\ tot} = R_{th\ j\text{-}c} + R_{th\ c\text{-}hs} + R_{th\ hs}$

$R_{th\ c\text{-}hs} + R_{th\ hs}$ = 25 – 4 = 21 K/W

CHARACTERISTICS

V_P = 12 V;T_{amb} = 25 °C; f_i = 1 kHz; R_L = 16 Ω; unless otherwise specified (see Fig.13).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	voltage supply		4.5	–	18.5	V
$I_{q(tot)}$	total quiescent current	V_P = 12 V; $R_L = \infty$; note 1	–	22	25	mA
Maximum gain; $V_{1,7} \geq$ 1.4 V						
P_{out}	output power	THD = 10%; R_L = 16 Ω	3.0	3.5	–	W
		THD = 10%; R_L = 8 Ω	–	5.3	–	W
THD	total harmonic distortion	P_{out} = 0.5 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(rms)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1	–	–	V
V_{no}	noise output voltage	f_i = 500 kHz; note 2	–	210	–	μV
B	bandwidth	at –1 dB	–	note 3	–	dB
SVRR	supply voltage ripple rejection	note 4	34	38	–	dB
$V_{O(os)}$	DC output offset voltage	$\|V_{13}-V_{11}\|$ and $\|V_{10}-V_8\|$	–	0	200	mV
Z_i	input impedance (pins 3 and 5)		15	20	25	kΩ
α_{cs}	channel separation	R_s = 5 kΩ	40	–	–	dB
$\|G_v\|$	channel unbalance	note 5	–	–	1	dB
		G_1 = 0 dB; note 6	–	–	1	dB
Mute position; $V_1 = V_7$ =0.4 V ±30 mV						
V_O	output voltage in mute position	V_I = 1.0 V; note 7	–	35	40	μV
DC volume control						
G_C	gain control range		68	73.5	–	dB
I_{DC}	volume control current	$V_1 = V_7$ = 0 V	–20	–25	–30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f_i = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. 20 Hz to 300 kHz (typical.
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
5. The channel unbalance is measured with $V_{DC1} = V_{DC2}$.
6. The channel unbalance at G_1 = 0 dB is measured with $V_{DC1} = V_{DC2}$.
7. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

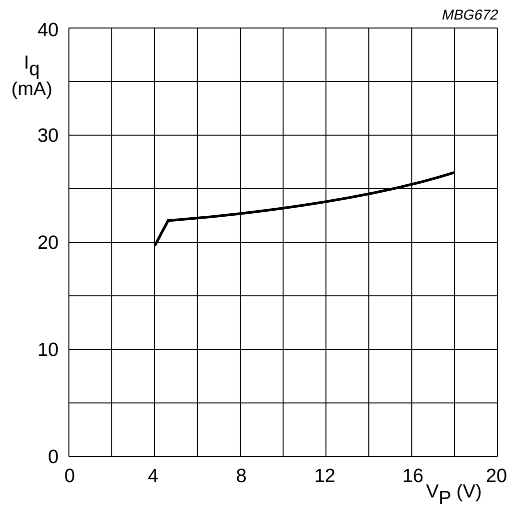
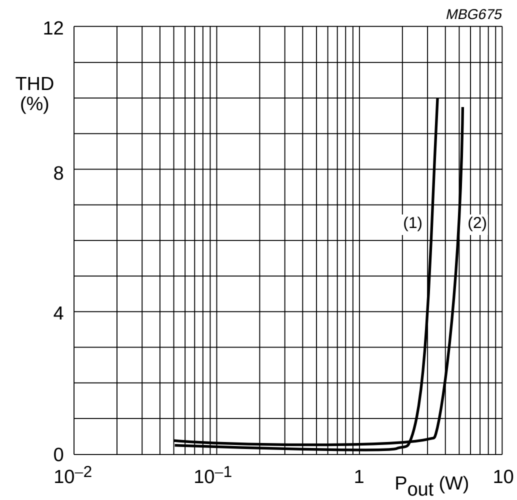
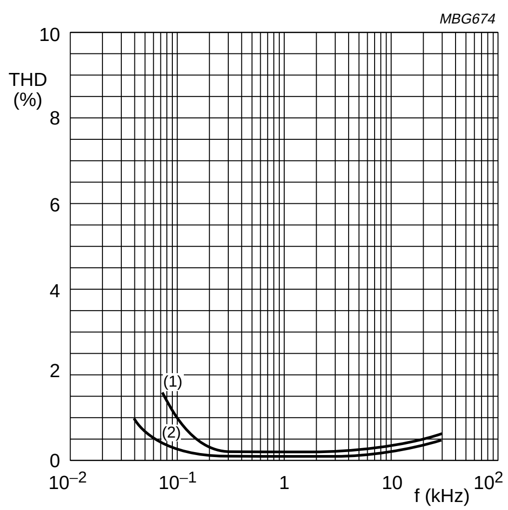


Fig.3 Quiescent current as a function of supply voltage.



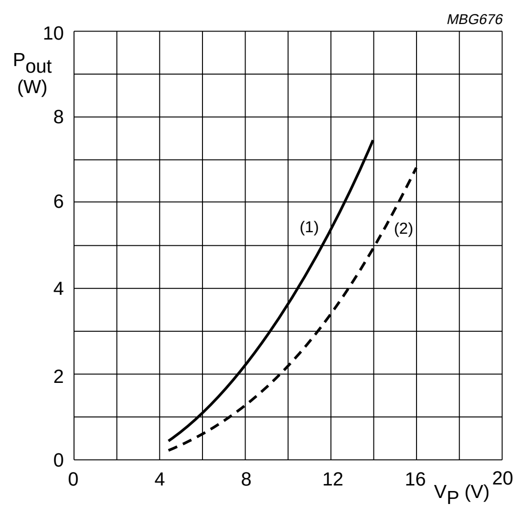
(1) R_L = 16 Ω.
(2) R_L = 8 Ω.

Fig.4 THD as a function of output power.



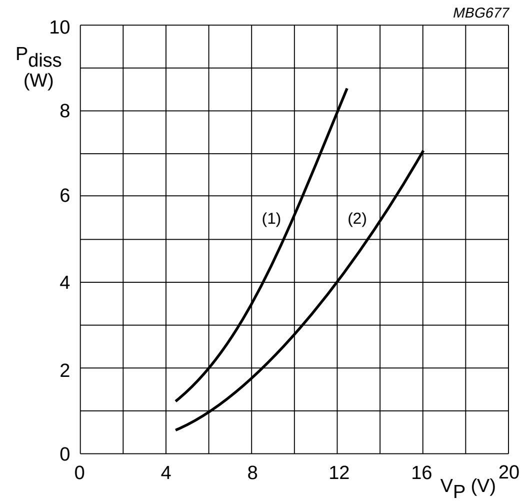
(1) G_v = 40 dB; P_o = 0.5 W.
(2) G_v = 30 dB; P_o = 0.5 W.

Fig.5 THD as a function of frequency.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.6 Output power as a function of supply voltage.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.7 Total worst case power dissipation as a function of supply voltage.

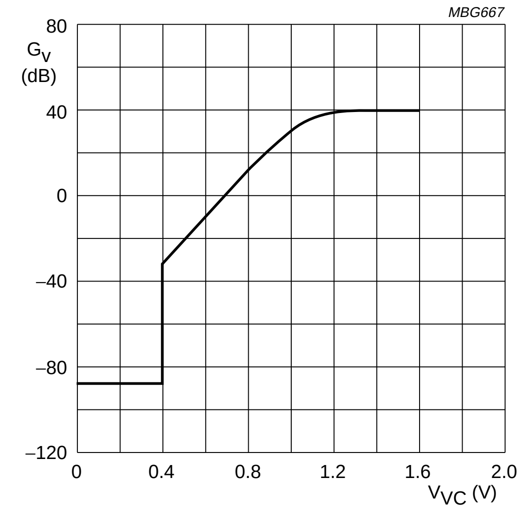
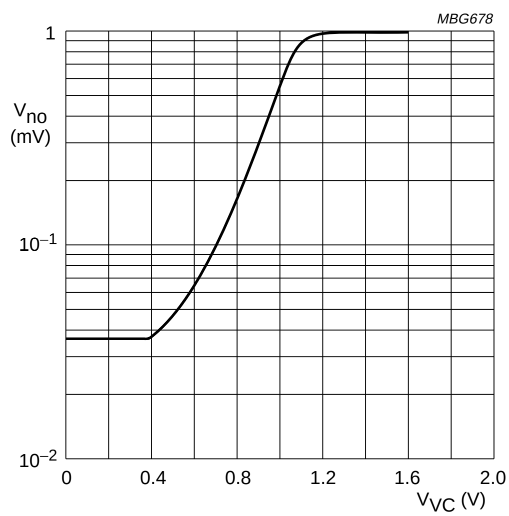
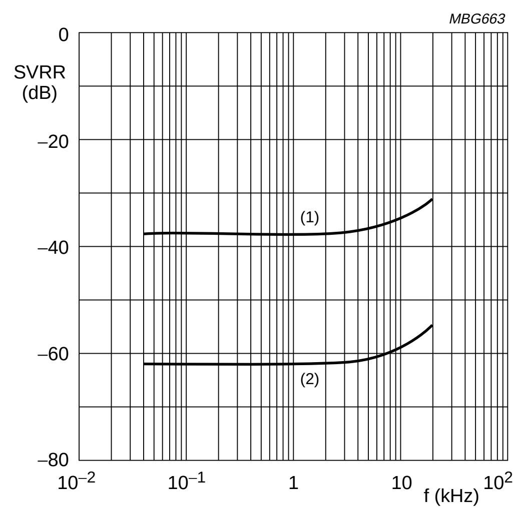


Fig.8 Voltage gain as a function of volume control voltage.



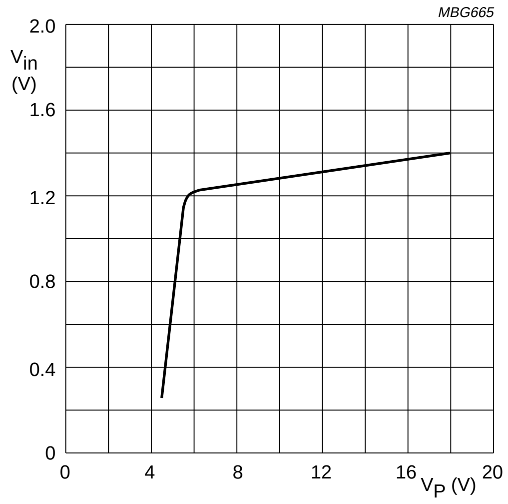
Frequency = 22 Hz to 22 kHz.

Fig.9 Noise voltage as a function of volume control voltage.



(1) V_{DC} = 1.4 V; V_{ripple} = 0.2 V.
(2) V_{DC} = 0.4 V; V_{ripple} = 0.2 V.

Fig.10 SVRR as a function of frequency.



THD = 1 %.

Fig.11 Input signal handling

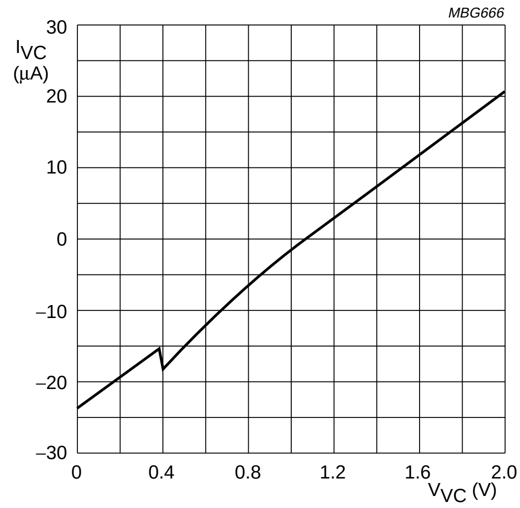


Fig.12 Volume control current as a function of volume control voltage.

APPLICATION INFORMATION

The application diagram is illustrated in Fig.13.

Test conditions

T_{amb} = 25 °C unless otherwise specified; V_P = 12 V; V_{DC} = 1.4 V; f_i = 1 kHz; R_L = 16 Ω.

The quiescent current has been measured without load impedance.

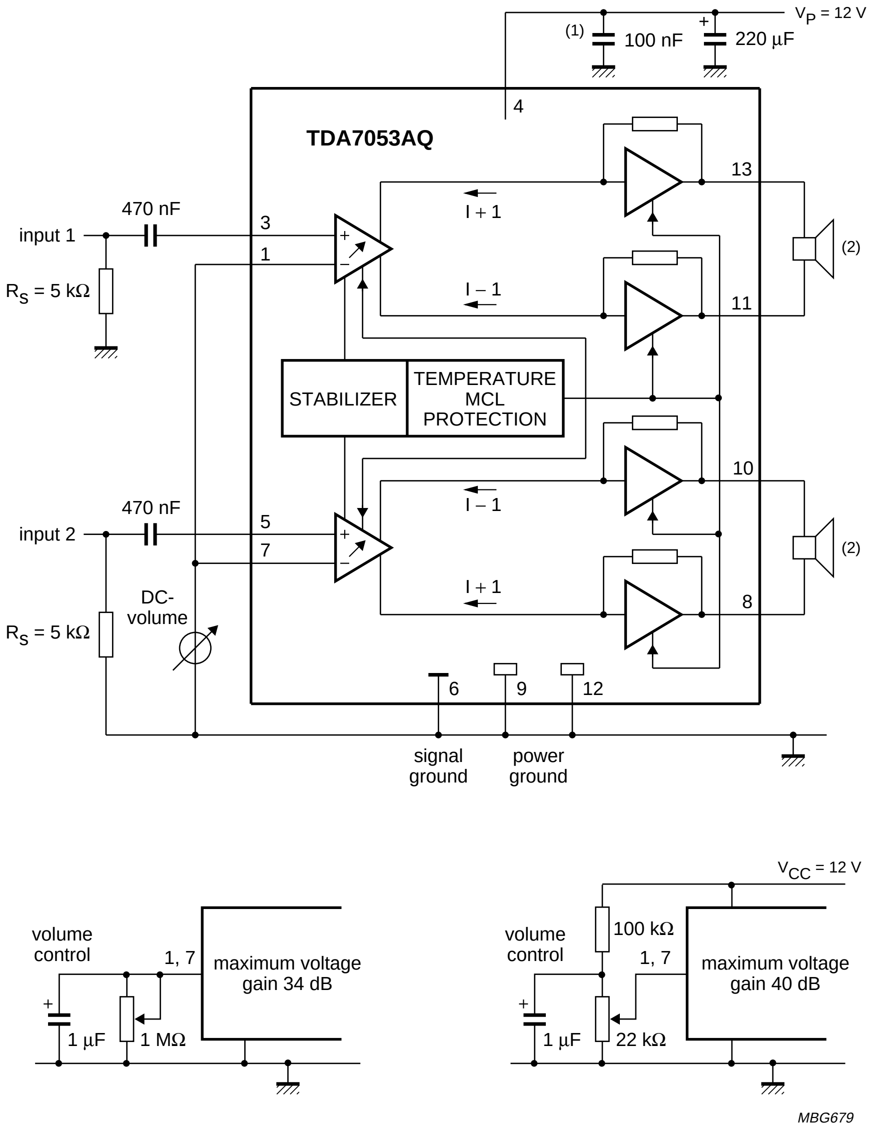
The output power as a function of the supply voltage has been measured at THD = 10%. The maximum output power is limited by the maximum power dissipation and the maximum available output current.

The maximum input signal voltage is measured at THD = 1% at the output with a voltage gain of 0 dB.

To avoid instabilities and too high a distortion, the input ground and power ground must be separated as far as possible and connected as close as possible to the IC.

The DC volume control can be applied in several ways. Two possible circuits are shown below the main application diagram. The circuits at the control pin will influence the switch-on and switch-off behaviour and the maximum voltage gain.

For single-end applications the output peak current must not exceed 100 mA. At higher output currents the short-circuit protection (MCL) will be active.



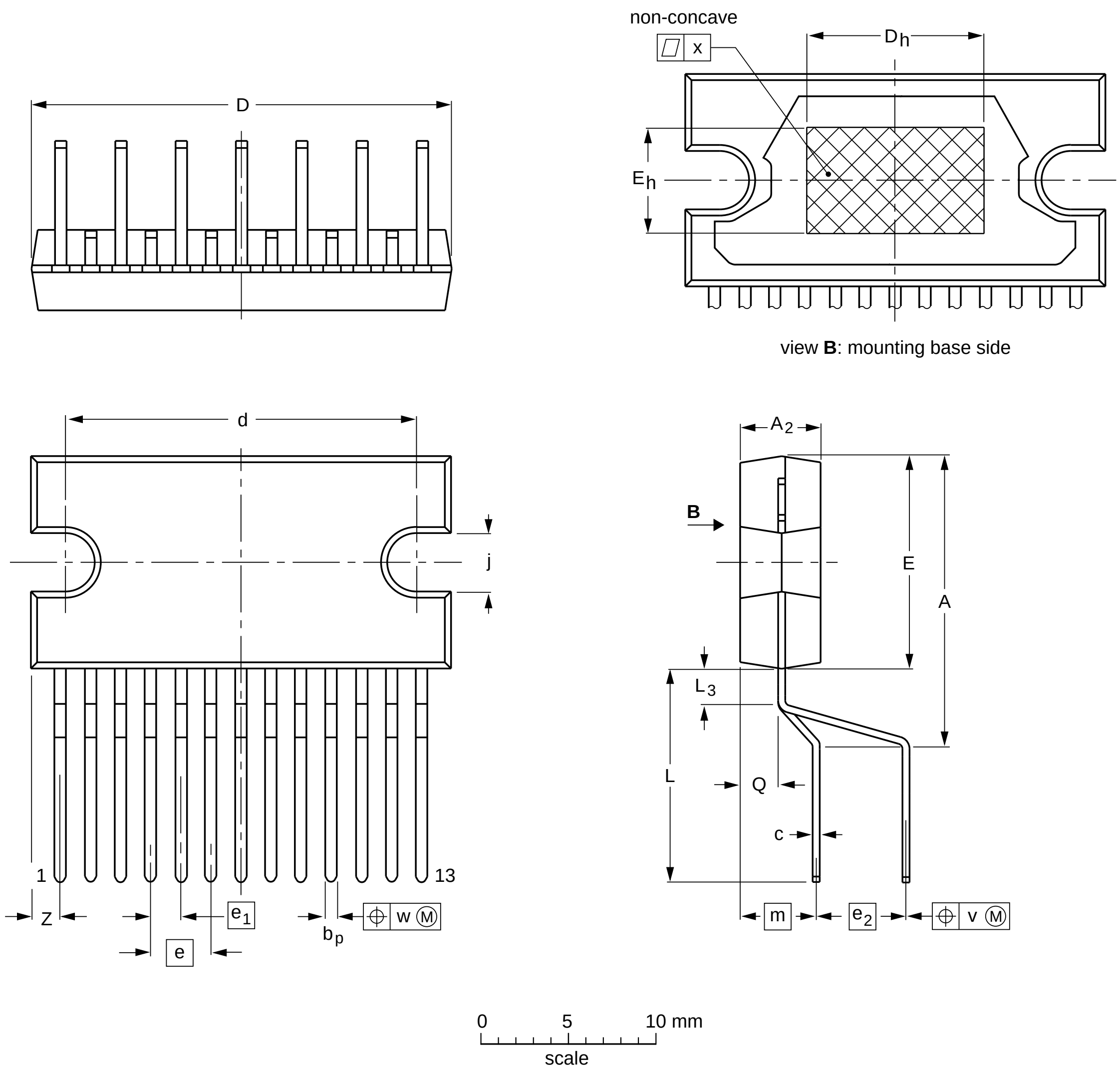
(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 5.

(2) R_L = 16 Ω.

Fig.13 Test and application diagram.

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	D(1)	d	D_h	E(1)	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	Z(1)
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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